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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/814,355	03/21/2001	Robert Warren Sherburne JR.		3657

38236 7590 09/20/2004

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EXAMINER	
CAO, CHUN	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 09/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/814,355	SHERBURNE, ROBERT WARRE	
	Examiner	Art Unit	
	Chun Cao	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *11-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892) ✓
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are presented for examination. Applicant withdraws claims 11-20.

2. The text of those applicable section of Title 35, U.S. Code not included in this action can be found in the prior Office Action.

Double Patenting

3. The non-statutory double patenting rejection, whether of the obviousness-type or non-obviousness-type, is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent, the possible harassment by multiple assignees, and the possibility that one might avoid the effect of file wrapper estoppel by filing a second application. *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); and *In re Goodman*, 29 USPQ2d 2010 (Fed. Cir. 1993).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) and © may be used to overcome an actual or provisional rejection based on a non-statutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1-3 rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-3 of copending Application No. 09/837,651. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are directed to substantially the same invention including one or more processing units and a clock controller varying the clock frequency to each processing unit. Although claims 1-3 of the copending Application do not recite the processor core including a memory, it is well known that processor core routinely include a memory unit.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

5. The terminal disclaimer filed on 6/8/2004 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of any patent granted on Application No. 09/837651 has been reviewed and is NOT accepted.

> The disclaimer fee of $110 in accordance with 37 CFR 1.20(d) has not been submitted, nor is there any authorization in the application file to charge a specified Deposit Account or credit card.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not

described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification fails to disclose that a low power reconfigurable processor core comprising a high-density memory array core coupled to the processor units. As shown in figure 5 and in specification pages 17-18, **ONLY** a device 100 comprises a low power reconfigurable core and a high-density memory array core.

8. Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitations "each unit" in line 2; "each controller" in line 5. There are insufficient antecedent basis for these limitations in the claim.

Claim 2 recites the limitations "the processor core" in line 1. There is insufficient antecedent basis for this limitation in the claim. The examiner interpreted "the processor core " as the low power reconfigurable processor core for examination purpose. Applicant is welcome to provide feed back in the next response to clarify the issue.

Claims 2-9 are rejected because they incorporate the deficiencies of claim 1.

9. Due to the number of 35 USC § 112, second paragraph rejections, the examiner has provided a number of examples of the claim deficiencies in the above rejection(s); however, the list of rejections may not be all inclusive. Applicant should refer to these rejection(s) as examples of deficiencies and should make all the necessary corrections to eliminate the 35 USC § 112, second paragraph problems and place the claims in a proper format.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 1, 2 and 4-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Ohmori (Ohmori), US patent no. 6,647,502.

The rejection for claims 1-10 are respectfully maintained to the extended that is applicable to the amended claims and reproduced hereinbelow for applicant's convenience.

As per claim 1, Ohmori discloses a low power a reconfigurable processor core [fig. 1, col. 8, lines 34-36], comprising:

a plurality of processor units [modules 4, 6, fig. 1; col. 1, lines 29-37; col. 4, lines 45-47;col. 8, lines 34-36], each processor unit having a clock input that controls the performance of each processor unit; one or more clock controllers [7, 8, fig. 1] having clock outputs each coupled to the clock inputs of the processor units [col. 3, lines 39-40, 52-54], each clock controller varying the clock frequency of each processor unit to optimize speed and processing power for a task [col. 3, line 64-col. 4, line 4; col. 9, lines 33-35, 44-47]; and

a high-density memory array core [3, 5, fig. 1] coupled to the processor units [col.

3, lines 26-27].

As per claim 2, inherently, Ohmori discloses that the low power reconfigurable processor core includes one or more digital signal processor [fig. 1; col. 8, lines 34-36, emphasis added "a processor...processes graphic data, audio data...].

As per claim 4, Ohmori discloses that the processor unit [modules 4, 6] includes a central processing unit (CPU) [col. 8, lines 34-36] having a clock input coupled to the clock controller; and a buffer [3, 5, fig. 1] adapted to be read by the CPU, the buffer having a clock input coupled to the clock controller [fig. 1; col. 3, lines 38-56; col. 8, lines 22-25].

As per claim 5, Ohmori discloses the CPU and the buffer are commonly clocked [fig. 1; col. 3, lines 38-41].

As per claim 6, Ohmori discloses the CPU and the buffer are separately clocked [fig. 1; col. 3, lines 38-56].

As per claim 7, Ohmori discloses that a second buffer adapted to receive data from the CPU, the second buffer having a clock input coupled to the clock controller [col. 3, lines 49-56; col. 8, lines 62-65].

As per claim 8, Ohmori discloses that the CPU, the buffer and the second buffer are commonly clocked [fig. 1; col. 3, lines 38-56].

As per claim 9, Ohmori discloses that the CPU, the buffer and the second buffer are separately clocked [fig. 1; col. 3, lines 38-56].

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 3 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohmori (Ohmori), US patent no. 6,647,502 in view of Nishiyama et al. (Nishiyama), US Patent no. 5,790,877.

As per claim 3, Ohmori fails to explicitly discloses the reconfigurable processor core includes one or more reduced instruction set computer (RISC) processors.

Nishiyama discloses one of the processing unit comprises a RISC processor [col. 3, lines 35-42].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of Ohmori and Nishiyama because they are both directed to the problem of reducing the power consumption of a processor core, and the specify teachings of Nishiyama stated above would have allowed for greater processing capabilities by using the RISC processor to improve the functionality of Ohmori's system.

As per claim 10, Nishiyama further discloses that the processor core comprises a private instruction random access memory coupled to the CPU; and a private data random access memory coupled to the CPU [fig. 1; col. 3, lines 45-50].

14. Applicant's arguments filed on 6/8/2004 have been fully considered but are not persuasive.

15. In the remarks, applicant argued in substance that Ohmori does not show a plurality of processor units, a high-density memory array core and there is no basis in the art for combining both Ohmori and Nishiyama references.

16. The examiner respectfully submits that applicant's position is not persuasive. The amended language of "processor units" is the same as the scope of the original language "processing units". And the applicant has not made the distinction between processor units and processing units, a high-density memory array core and FIFOs. Therefore, the scope of amended language is the same as the scope of the original language. Also, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Ohmori fails to disclose RISC processors. However, Nishiyama discloses RISC processor [col. 3, lines 35-42]. It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of Ohmori and Nishiyama because they are both directed to the problem of reducing the power consumption of a processor core, and the specify teachings of Nishiyama stated above would have allowed for greater processing capabilities by using the RISC processor to improve the functionality of Ohmori's system.

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hara et al., US patent no. 5,724,591, discloses a multiprocessor system comprises a plurality of processor units and a main memory is connected to the processor units [fig. 1; col. 4, lines 32-51].

Van Der Wal et al., US patent no. 6,188,381 discloses a processing module containing a general purpose microprocessor [abstract all].

18. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao at (703) 308-6106 (571-272-3664, effective 10/14/2004). The examiner can normally be reached on Monday-Friday from 7:30 am - 4:00 pm. If attempts to reach the examiner by phone are unsuccessful, the examiner's supervisor Thomas Lee can be reached at (703) 305-9717 (571-272-3667, effective 10/14/2004). The fax number for this Art Unit is following: Official (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 306-5631 (571-272-2100, effective 10/14/2004).

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Chun Cao

Sep. 14, 2004